

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

5 **Patent Application**

Applicant(s): Dwyer et al.

Case: 5-13

Serial No.: 09/975,764

10 Filing Date: October 9, 2001

Group: 2185

Examiner: John A. Lane

Title: Method and Apparatus for Adaptive Cache Frame Locking and Unlocking

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REPLY BRIEF

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Mail Stop Appeal Brief – Patents

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

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Sir:

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Appellants hereby reply to the Examiner's Answer, mailed October 20, 2006  
(referred to hereinafter as "the Examiner's Answer"), in an Appeal of the final rejection of claims  
1-36 in the above-identified patent application.

REAL PARTY IN INTEREST

A statement identifying the real party in interest is contained in Appellants' Appeal

35 Brief.

RELATED APPEALS AND INTERFERENCES

A statement identifying related appeals is contained in Appellants' Appeal Brief.

STATUS OF CLAIMS

A statement identifying the status of the claims is contained in Appellants' Appeal Brief. Claims 1-8 and 11-36 are being appealed.

STATUS OF AMENDMENTS

A statement identifying the status of the amendments is contained in Appellants' Appeal Brief.

SUMMARY OF CLAIMED SUBJECT MATTER

A Summary of the Invention is contained in Appellants' Appeal Brief.

STATEMENT OF GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A statement identifying the grounds of rejection to be reviewed on appeal is contained in Appellants' Appeal Brief.

CLAIMS APPEALED

A copy of the appealed claims is contained in an Appendix of Appellants' Appeal Brief.

ARGUMENT

Independent claims 1, 15, 23, and 29 are rejected under 35 U.S.C. §103(a) as being unpatentable over the admitted prior art in view of Malamy et al. In particular, the Examiner asserts that the admitted prior art teaches the claimed step of "locking frames if a task is interrupted by another task." The Examiner acknowledges that the admitted prior art does not discuss locking a frame or frames in accordance with a most recently used scheme, but asserts that Malamy teaches locking pages or blocks in the cache in accordance with a most recently used locking scheme. In the Examiner's Answer, the Examiner alleges that the applicant did not consider the benefits of both prior art devices working in concert, and contends that each prior art device working together would lock the most recently used frames of a task.

First, Appellants note that the admitted prior art teaches to lock all frames associated with a task, if the task is interrupted by another task. Independent claims 1 and 29

require locking a number of most recently used frames *associated with a task*. Independent claims 15 and 23 require locking said number of said most recently used frames *if a task is interrupted by another task*. Thus, the admitted prior art actually *teaches away* from the present invention by teaching to lock **all** frames associated with a task.

5 Appellants also note that Malamy teaches a scheme that prevents the most recently used lines in a cache from being replaced when the cache controller is forced to replace a cache memory line. The most recently used cache lines are thus blocked from being replaced, *regardless of the task they are associated with and regardless of whether a task is interrupted by another task*. The present invention, alternatively, recognizes that the most recently accessed frames in a cache  
10 memory are likely to be accessed by a task again in the near future. Thus, the most recently used frames *associated with a task* may be locked in accordance with the present invention at the beginning of a task switch or interrupt, and are thus available when an interrupted task resumes execution (to improve the performance of the cache). Independent claims 1 and 29 require locking a number of most recently used frames *associated with a task*. Independent claims 15 and 23  
15 require locking said number of said most recently used frames *if a task is interrupted by another task*. Malamy, therefore, actually *teaches away* from the present invention by teaching to block the replacement of the most recently used cache lines ***regardless of the task they are associated with***

Thus, the admitted prior art and Malamy, alone or in combination, do not disclose  
20 or suggest locking a number of most recently used frames associated with a task, as required by independent claims 1 and 29, and do not disclose or suggest locking said number of said most recently used frames if a task is interrupted by another task, as required by independent claims 15 and 23.

Furthermore, Appellants could find no disclosure or suggestion in the prior art to  
25 combine the prior art techniques cited by the Examiner. Regarding the Examiner's allegation that the applicant did not consider the benefits of both prior art devices working in concert, Appellants note that, as stated above, each of the cited prior art disclosures actually teaches away from the present invention. Thus, a person of ordinary skill in the art would not look to combine Malamy and the admitted prior art.

Claims 5-7, 11, 13, 18-21, 24, 25, 27, 31 and 34-36

Claims 5/18, 6/19/24/34, 7/20, 11/21/25/31/35, and 13/27/36 specify a number of limitations providing additional bases for patentability. Specifically, the Examiner rejected the cited claims under 35 U.S.C. §103(a) as being unpatentable over the admitted prior art in view of

5 Malamy et al. Claims 5 and 18 require an identifier of the  $n$  most recently used frames is maintained for each of a plurality of tasks. Claims 6, 19, 24, and 34 require not locking all the frames in a set concurrently. Claims 7 and 20 require wherein said number of said most recently used frames identifies the most recently accessed  $3n/2$  frames on average. Claims 11, 25, 31, and 35 require an adaptive frame unlocking mechanism that automatically unlocks frames that cause a

10 performance degradation for a task. Claims 13 and 36 require wherein said cache is a two way set associative cache and said most recently used frames are identified by taking an inverse of a least recently used identifier.

Regarding the dependent claims, the Examiner asserts that it is believed that most, if-not-all, dependent claim features are taught by the admitted prior art and/or Malamy. In the

15 Examiner's Answer, the Examiner asserts that, regarding claims 5 and 18, the admitted prior art essentially teaches the concept of associating frames with one of a plurality of tasks (citing page 2 of the specification). Regarding claims 6, 19, 24, and 34, the Examiner contends the frames in either the admitted prior art or Malamy can be locked over time (i.e. not concurrently) as needed and that Malamy's device determines which MRU frames/lines/blocks to lock over time.

20 Regarding claims 7 and 20, the Examiner asserts that a value of  $2/3$  for  $n$  would yield 1 in the equation  $3n/2$  and contends that Malamy teaches at least 1 most recently used frame or most recently accessed frame on average. Regarding claims 11, 25, 31, and 35, the Examiner asserts that Malamy teaches resetting a lock bit in accordance with a locking scheme that controls the state of lock bits based upon the intelligence and knowledge of frequency of use of certain memory

25 locations to provide a more efficient cache (see, Abstract). Regarding claims 13 and 36, the Examiner asserts that

Malamy teaches a Pseudo-Least-Recently-Used (PLRU) scheme that uses a MRU bit that indicates the cache memory line has been used recently (col 3, lines 6-19). Thus, a set LRU bit would not identify the most recently used (MRU) frame/block/line and a set MRU bit would not identify the least recently used (LRU) frame/block/line. Furthermore, Malamy (see Summary) discusses fully associative, set associative and direct mapped caches. A two way set associative cache is inherently within the scope of Malamy's invention.

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Regarding claims 5 and 18, the Examiner asserts that the admitted prior art essentially teaches the concept of associating frames with one of a plurality of tasks (citing page 2 of the specification). Appellants note that the admitted prior art, however, does not disclose or suggest an *identifier of the n most recently used frames is maintained* for each of a plurality of tasks

Regarding claims 6, 19, 24, and 34, the Examiner contends the frames in either the admitted prior art or Malamy can be locked over time (i.e. not concurrently) as needed and that Malamy's device determines which MRU frames/lines/blocks to lock over time. This assertion, however, is *not equivalent to the limitation of the cited claims*, which require *not locking all the frames in a set concurrently*.

Regarding claims 7 and 20, the Examiner asserts that a value of  $2/3$  for  $n$  would yield 1 in the equation  $3n/2$  and contends that Malamy teaches at least 1 most recently used frame or most recently accessed frame on average. In the Examiner's Answer dated December 4, 2006, the Examiner asserts that the variable " $n$ " is not defined in claims 7 and 20, and that the cited claims are therefore indefinite.

Appellants note that *n is defined as an integer* in the present specification (see, page 4, lines 1-11, and page 6, lines 10-17, of the originally filed specification) and as would be apparent to a person of ordinary skill in the art. Thus,  $n$  may not equal  $2/3$ . Regarding the Examiner's assertion that claims 7 and 20 are indefinite, Appellants note that there is currently no section 112 rejection pending. Although the variable " $n$ " is sufficiently defined in the specification, Appellants propose to add language to clarify the definition of the variable " $n$ " in the claims upon resolution of the appeal.

Regarding claims 11, 25, 31, and 35, the Examiner asserts that Malamy teaches resetting a lock bit in accordance with a locking scheme that controls the state of lock bits based upon the intelligence and knowledge of frequency of use of certain memory locations to provide a more efficient cache (see, Abstract). This assertion, however, is *not equivalent to the limitation of the cited claims*, which requires an adaptive frame unlocking mechanism that automatically unlocks frames that *cause a performance degradation for a task*.

Regarding claims 13 and 36, the Examiner asserts that Malamy teaches a set LRU bit that would not identify the most recently used (MRU) frame/block/line and a set MRU bit would not identify the least recently used (LRU) frame/block/line. This assertion, however, is *not*

*equivalent to the limitation of the cited claims, which requires wherein said cache is a two way set associative cache and said most recently used frames are identified by **taking an inverse** of a least recently used identifier.*

Thus, the admitted prior art and Malamy (alone or in combination) do not disclose or suggest an identifier of the  $n$  most recently used frames is maintained for each of a plurality of tasks, as required by claims 5 and 18, do not disclose or suggest not locking all the frames in a set concurrently, as required by claims 6, 19, 24, and 34, do not disclose or suggest wherein said number of said most recently used frames identifies the most recently accessed  $3n/2$  frames on average, as required by claims 7 and 20, do not disclose or suggest an adaptive frame unlocking mechanism that automatically unlocks frames that cause a performance degradation for a task, as required by claims 11, 25, 31, and 35, and do not disclose or suggest wherein said cache is a two way set associative cache and said most recently used frames are identified by taking an inverse of a least recently used identifier, as required by claims 13 and 36.

#### Conclusion

The rejections of the cited claims under section 103 in view of the admitted prior art and Malamy are therefore believed to be improper and should be withdrawn. The remaining rejected dependent claims are believed allowable for at least the reasons identified above with respect to the independent claims.

The attention of the Examiner and the Appeal Board to this matter is appreciated.

Respectfully,



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APPENDIX

1. A cache memory, comprising:
  - a plurality of cache frames for storing information from main memory; and
  - 5 an adaptive frame locking mechanism for locking a number of most recently used frames associated with a task.
2. The cache memory of claim 1, further comprising a memory for recording an identifier of the n most recently used frames.
- 10 3. The cache memory of claim 2, wherein said identifier is a frame address.
4. The cache memory of claim 2, wherein said identifier is a flag associated with said most recently used frames
- 15 5. The cache memory of claim 2, wherein said identifier of the n most recently used frames is maintained for each of a plurality of tasks.
6. The cache memory of claim 1, wherein said adaptive frame locking mechanism does not lock  
20 all the frames in a set concurrently.
7. The cache memory of claim 1, wherein said number of said most recently used frames identifies the most recently accessed  $3n/2$  frames on average.
- 25 8. The cache memory of claim 1, wherein said adaptive frame locking mechanism includes three latches (a, b, and lock) for each frame of said cache.
9. The cache memory of claim 8, wherein said latch a is set when a frame is accessed and the value in latch a of a frame is transferred to latch b and latch a is reset after n accesses.
- 30 10. The cache memory of claim 8, wherein said adaptive frame locking mechanism sets a lock latch of a given frame, locking the frame, if either latch a or latch b is set when the lock signal is

asserted.

11. The cache memory of claim 1, further comprising an adaptive frame unlocking mechanism that automatically unlocks frames that cause a performance degradation for a task.

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12. The cache memory of claim 11, wherein said adaptive frame unlocking mechanism includes a counter for monitoring a number of times a task experiences a frame miss.

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13. The cache memory of claim 1, wherein said cache is a two way set associative cache and said most recently used frames are identified by taking an inverse of a least recently used identifier.

14. The cache memory of claim 1, wherein said locking is performed if a first task is interrupted by a second task.

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15. A method for locking frames in a cache memory, said method comprising the steps of:  
     storing information from main memory in frames of said cache memory;  
     monitoring a number of most recently used frames; and  
     locking said number of said most recently used frames if a task is interrupted by another task.

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16. The method of claim 15, wherein said monitoring step maintains a frame address of said most recently used frames.

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17. The method of claim 15, wherein said monitoring step maintains a flag associated with said most recently used frames.

18. The method of claim 15, wherein said monitoring step maintains an identifier of the n most recently used frames for each of a plurality of tasks.

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19. The method of claim 15, wherein said locking step does not lock all the frames in a set concurrently.

20. The method of claim 15, wherein said number of said most recently used frames identifies the most recently accessed  $3n/2$  frames on average.

21. The method of claim 15, further comprising the step of automatically unlocking frames that cause a significant performance degradation for a task.

22. The method of claim 21, wherein said step of unlocking further comprises the step of monitoring a number of times a task experiences a frame miss.

23. A cache memory comprising:

a memory element for storing information from main memory in frames of said cache memory;

means for monitoring a number of most recently used frames; and

means for locking said number of said most recently used frames if a task is interrupted by another task.

24. The cache memory of claim 23, wherein said means for locking said frames does not lock all the frames in a set concurrently.

25. The cache memory of claim 23, further comprising means for unlocking said locked frames that automatically unlocks frames that cause a significant performance degradation for a task.

26. The cache memory of claim 25, wherein said means for unlocking includes a counter for monitoring a number of times a task experiences a frame miss.

27. The cache memory of claim 23, wherein said cache is a two way set associative cache and said most recently used frames are identified by taking an inverse of a least recently used identifier.

28. The cache memory of claim 23, wherein said locking is performed if a first task is interrupted by a second task.

29. An integrated circuit, comprising:

a cache memory having a plurality of cache frames for storing information from main memory; and

5 an adaptive frame locking mechanism for locking a number of most recently used frames associated with a task.

30. The integrated circuit of claim 29, further comprising a memory for recording an identifier of the n most recently used frames.

10 31. The integrated circuit of claim 29, further comprising an adaptive frame unlocking mechanism that automatically unlocks frames that cause a performance degradation for a task.

32. The integrated circuit of claim 29, wherein said locking is performed if a first task is interrupted by a second task.

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33. A cache memory device comprising:

a memory element for storing information from main memory in frames of said cache memory device;

a monitor for monitoring a number of most recently used frames; and

20 an adaptive frame locking mechanism for locking said number of said most recently used frames if a task is interrupted by another task.

34. The cache memory device of claim 33, wherein said adaptive frame locking mechanism does not lock all the frames in a set concurrently.

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35. The cache memory device of claim 33, wherein said adaptive frame locking mechanism automatically unlocks frames that cause a significant performance degradation for a task.

36. The cache memory device of claim 33, wherein said cache is a two way set associative cache and said most recently used frames are identified by taking an inverse of a least recently used identifier.

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EVIDENCE APPENDIX

There is no evidence submitted pursuant to § 1.130, 1.131, or 1.132 or entered by the Examiner and relied upon by appellant.

RELATED PROCEEDINGS APPENDIX

There are no known decisions rendered by a court or the Board in any proceeding identified pursuant to paragraph (c)(1)(ii) of 37 CFR 41.37.